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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/888,717	06/25/2001	Jerrell Hein	026-0006	8760

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EXAMINER	
AHN, SAM K	

ART UNIT	PAPER NUMBER
2637	

DATE MAILED: 01/23/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/888,717	HEIN ET AL.	
	Examiner	Art Unit	
	Sam K. Ahn	2637	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *07 November 2005*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-25* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-7,10-19 and 22-25* is/are rejected.

7)☒ Claim(s) *8,9,20 and 21* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Response to Arguments

1. Applicant's arguments filed 11/07/05 have been fully considered but they are not persuasive. On p.7-11 applicants argue that Tamamura in view of Suzuki do not teach all the limitations claimed in claims 1,15 and 24. The examiner respectfully disagrees. Applicants argue that Tamamura does not teach "a phase detector circuit coupled to generate a difference signal indicating a phase difference between an incoming data stream and a delayed clock signal". The examiner explains that Tamamura teaches a phase detector circuit (201-1) coupled to generate a difference signal (201a-1) indicating a phase difference between an incoming data stream (11-1) and a delayed clock signal (204a-1). It appears that the applicants do not agree that the frequency divider (204-1 in Fig.4 of Tamamura) outputting the delayed clock signal (204a-1) is not actually the delayed clock signal.

The examiner cites Nair et al. US 6,229,357 B1 teaching a frequency divider (see Fig.4) further comprising delay elements (see 420,430). Therefore, it is inherent that a frequency divider includes delay elements in order to produce the delayed clock signal.

Applicants further argue that Tamamura in view of Suzuki does not teach the limitation of the output of the delay device (7 of Suzuki) is provided to an internal circuit (6), thus do not teach the limitation of a phase detector circuit coupled to generate a difference signal indicating a phase difference between an incoming data stream and the delayed clock signal, the delayed clock signal being provided based

on a delay control signal derived from the difference signal. The examiner respectfully disagrees.

Suzuki teaches a clock delay circuit (7 in Fig.1) coupled to receive a delay control signal (107) derived from the difference signal (108) and to receive the output clock signal (105), the clock delay circuit (7) coupled to provide as the delayed clock signal an output clock signal (106) delayed according to the delay control signal (107, note col.4, lines 20-27).

Therefore, it would have been obvious to one skilled in the art at the time of the invention to incorporate the teaching of Suzuki in the system of Tamamura by providing the delay control signal (202a-1) to the clock delay circuit (204-1), as taught by Suzuki wherein the delay control signal (107) is provided to the clock delay circuit (7), for the purpose of designing a flexible and robust system by adding a function of controlling the delay time in the clock delay circuit (note col.4, lines 38-48, Suzuki).

Although Suzuki teaches wherein the delay device 7 (clock delay circuit) of Suzuki provides its output to an internal circuit 6, the output of the clock delay circuit may be provided to the phase comparator (204-1 providing output to the phase comparator 201-1), as taught by Tamamura. Hence, a more controlled delayed signal would be provided to the phase comparator of Tamamura.

Regarding claim 14, in response to applicant's argument that there is no suggestion to combine the references, the examiner recognizes that obviousness can only be

established by combining or modifying the teachings of the prior art to produce the claimed invention where there is some teaching, suggestion, or motivation to do so found either in the references themselves or in the knowledge generally available to one of ordinary skill in the art. See *In re Fine*, 837 F.2d 1071, 5 USPQ2d 1596 (Fed. Cir. 1988)and *In re Jones*, 958 F.2d 347, 21 USPQ2d 1941 (Fed. Cir. 1992). In this case, Bulzachelli teaches the limitation of having an explicit zero in a closed loop (note col.3, lines 20-32). Therefore, it would have been obvious to one skilled in the art at the time of the invention to incorporate the teaching of Bulzachelli in the system of Tamamura in view of Suzuki for the purpose of providing a loop stability, as taught by Bulzachelli. A stable system is always desired in any system to ensure that the system processes as intended. Hence, in order to increase the loop stability in the system of Tamamura in view of Suzuki, one skilled in the art may incorporate the teaching of Bulzachelli by providing the integrator and other circuitry, as taught by Bulzachelli.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

2. Claims 1-7,11,15-17 and 24 are rejected under 35 U.S.C. 103(a) as being unpatentable over Tamamura et al. USP 6,118,316 (Tamamura, cited previously) in view of Suzuki USP 6,353,648 B1 (cited previously).

Regarding claims 1,15 and 24, Tamamura teaches a clock recovery circuit (see Fig.4) comprising: a phase detector circuit (201-1) to generate a difference signal (201a-1) indicating a phase difference between an incoming data stream (11-1) and a delayed clock signal (201a-1); an oscillator circuit (203-1) responsive to a control signal (202a-1) derived from the difference signal (201a-1) to generate an output clock signal (output of 203-1) variable according to the control signal; and a clock delay circuit (204-1) coupled to receive the output clock signal.

However, Tamamura does not teach the clock delay circuit receiving a delay control signal derived from the difference signal and provide as the delayed clock signal the output clock signal delayed according to the delay control signal.

Suzuki teaches a clock delay circuit (7 in Fig.1) coupled to receive a delay control signal (107) derived from the difference signal (108) and to receive the output clock signal (105), the clock delay circuit (7) coupled to provide as the delayed clock signal an output clock signal (106) delayed according to the delay control signal (107, note col.4, lines 20-27).

Therefore, it would have been obvious to one skilled in the art at the time of the invention to incorporate the teaching of Suzuki in the system of Tamamura by providing the delay control signal (202a-1) to the clock delay circuit (204-1) for the purpose of designing a flexible and robust system by adding a function of

controlling the delay time in the clock delay circuit (note col.4, lines 38-48, Suzuki).

Regarding claim 2, Tamamura in view of Suzuki teach all subject matter claimed, as applied to claim 1. Tamamura further teaches comprising a loop filter (202-1) coupled to receive the difference signal and supply a filtered output as the control signal.

Regarding claims 3 and 16, Tamamura in view of Suzuki teach all subject matter claimed, as applied to claim 1 or 15. Tamamura further teaches wherein the control signal (202a-1) for the oscillator circuit (203-1) is used as the delay control signal (provided to 204-1).

Regarding claims 4 and 17, Tamamura in view of Suzuki teach all subject matter claimed, as applied to claim 1 or 15. Suzuki further teaches a delay control filter circuit (4) coupled to receive the difference signal (108) and generate the delay control signal (107) based thereon.

Regarding claims 5-7, Tamamura in view of Suzuki teach all subject matter claimed, as applied to claim 1. Suzuki further teaches wherein the clock delay circuit (7) is a voltage controlled delay circuit (see Fig.2 and note col.4, lines 34-42) and comprises multiple stages (by having plurality of inverters, 10), and

wherein a delay period from one stage to a next stage in the clock delay circuit is less than one period of the output clock signal (note col.4, lines 39-42 wherein the total delay time is adjusted by controlling each of the inverters).

Regarding claim 11, Tamamura in view of Suzuki teach all subject matter claimed, as applied to claim 1. Tamamura further teaches wherein the oscillator circuit is a voltage controlled oscillator (203-1, note col.8, lines 11-18).

3. Claims 10,12,13,18,19,22,23 and 25 are rejected under 35 U.S.C. 103(a) as being unpatentable over Tamamura et al. USP 6,118,316 (Tamamura, cited previously) in view of Suzuki USP 6,353,648 B1 (cited previously) and Kaylani et al. USP 6,711,227 B1 (Kaylani, cited previously).

Regarding claims 10,12,13,18,22,23 and 25 Tamamura in view of Suzuki teach all subject matter claimed, as applied to claim 1,15 or 24. However, Tamamura in view of Suzuki do not teach a first in first out (FIFO) memory coupled to write data into the FIFO memory with the delayed clock signal and to read data out of the FIFO memory with the output clock signal, thereby retiming data to the output clock signal.

Kaylani teaches a data recovery circuit in a FIFO memory (50 in Fig.5) coupled to write data into the FIFO memory with a clock signal (20) and to read data out of the FIFO memory with the output clock signal (16, output of a PLL having a phase detector), thereby retiming data to the output clock signal. And although

Kaylani does not explicitly teach the clock signal is the delayed clock signal, it would have been obvious to one skilled in the art at the time of the invention to write to the FIFO memory using the delayed clock signal for the purpose of synchronizing the FIFO memory to the delayed clock signal, which has been adjusted, thus receive a more synchronous signal.

And further, it would have been obvious to one skilled in the art at the time of the invention to incorporate the teaching of Kaylani of having the data recovery circuit comprising the FIFO memory in the system of Tamamura for the purpose of recovering data with through the clock recovery in the case of receiving signals, such as Manchester coded signals wherein data and clock are combined into the signal, thus synchronize the system based on the received signal.

Regarding claims 19, Tamamura in view of Suzuki teach all subject matter claimed, as applied to claim 18. Suzuki further teaches wherein the clock delay circuit (7) is a voltage controlled delay circuit (see Fig.2 and note col.4, lines 34-42) and comprises multiple stages (by having plurality of inverters, 10), and wherein a delay period from one stage to a next stage in the clock delay circuit is less than one period of the output clock signal (note col.4, lines 39-42 wherein the total delay time is adjusted by controlling each of the inverters).

4. Claim 14 is rejected under 35 U.S.C. 103(a) as being unpatentable over Tamamura et al. USP 6,118,316 (Tamamura, cited previously) in view of Suzuki USP 6,353,648 B1 (cited previously) and Bulzachelli (cited previously in the IDS).

   Regarding claim 14, Tamamura in view of Suzuki teach all subject matter claimed, as applied to claim 1. Tamamura further teaches a closed loop (20A in Fig.4), however, do not explicitly teach having the closed loop response without an explicit zero. Bulzachelli also teaches a phase detector (see 102 and 202 in Figs. 1 and 2) having a closed loop response and further teaches the loop amplifier and filter having an integrator plus other circuitry and contains an explicit zero. Therefore, it would have been obvious to one skilled in the art at the time of the invention to incorporate the teaching of Bulzachelli in the system of Tamamura having the integrator and other circuitry to provide an explicit zero for the purpose of providing a loop stability, as taught by Bulzachelli (note col.3, lines 20-32).

Allowable Subject Matter

5. Claims 8,9,20 and 21 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Conclusion

6. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Nair et al. US 6,229,357 B1 teach a frequency divider comprising delay elements.

7. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Sam Ahn whose telephone number is (571) 272-3044. The examiner can normally be reached on Monday-Friday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Jay Patel can be reached on (571) 272-2988. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Sam K. Ahn
1/19/06

YOUNG T. TSE
PRIMARY EXAMINER